LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a display device, and more particularly, to a liquid crystal display (LCD) device and a method for driving the same.

Background of the Related Art

[0002] In general, electromagnetic interference (EMI) means that electromagnetic waves directly or indirectly emitted from electronic appliances generate problems in an electromagnetic receiving function of other electronic appliances.

[0003] With an increasing number of various electronic appliances and the development of digital and semiconductor technologies, the utilization of precision electronic appliances proliferates, thereby generating large quantities of electromagnetic waves. Such electromagnetic waves cause EMI, operational failures of electronic appliances, and biological hazards.

[0004] The EMI has been an issue in LCD components of display devices. Particularly, it becomes increasingly necessary to reduce the EMI in LCD devices because the EMI degrades the display quality that is one of the most important elements in the display.

[0005] In general, an LCD includes two glass substrates, and a liquid crystal layer between the two glass substrates. In a thin film transistor (TFT) LCD, the TFT serves as a switching device that applies a signal voltage to the liquid crystal layer. The TFT LCD has attracted attention as a display device to substitute for a cathode ray tube (CRT) due to the LCD's low power consumption and portability.

[0006] As shown in FIG. 1, the TFT-LCD includes a lower substrate 1 having the TFT serving as the switching device, and an upper substrate 2 has a color filter. A liquid crystal is injected between the lower and upper substrates 1 and 2. The TFT-LCD can display a picture image by manipulating the electro-optical characteristics of the liquid crystal.

[0007] As also shown in FIG. 1, a TFT array region 4 is formed on the lower glass substrate 1. Then, a black matrix film 5, the color filter 6, a common electrode 7, and an alignment film 8 are formed on the upper glass substrate 2.

[0008] The lower and upper glass substrates 1 and 2 are attached to each other by a sealant such as an epoxy resin. A driving circuit 11 on a printed circuit board (PCB) 10 is connected to the lower glass substrate 1 through a tape carrier package (TCP) 12.

[0009] In a timing controller of the above described LCD device, a data signal is synchronized with a data clock signal DCLK, and then is provided to a source driver.

[0010] A related art LCD device will be described with reference to the accompanying drawings.

[0011] FIG. 2 is a structure view of a related art LCD device.

[0012] As shown in FIG. 2, the related art LCD device includes an LCD panel 21, source drivers 23, gate drivers 25, and a timing controller 27.

[0013] The source drivers 23 apply data signals to the LCD panel 21, and the gate drivers 25 apply gate driving signals to the LCD panel 21. The timing controller 27 outputs power supply and control signals for controlling the source and gate drivers, makes clock signals CLK by receiving a data clock signal DCLK and digital data from a system (not shown), and outputs data synchronized with the clock signals CLK to the source drivers 23.

[0014] At this time, the timing controller 27 provides the digital data input from the system to each source driver 23 through data buses DB. The timing controller 27 simultaneously provides the clock signals CLK to each source driver 23.

[0015] The LCD panel 21 displays a picture image by controlling the source and gate drivers 23 and 25. The LCD panel 21 includes a plurality of gate and data lines that cross, and the TFT and a pixel electrode are formed at the crossing point of the data and gate lines.

[0016] The TFT includes a gate electrode formed on the lower glass substrate, a gate insulating film formed on an entire surface of the lower glass substrate including the gate electrode, a semiconductor film formed on the gate insulating film above the gate electrode, and source and drain electrodes formed on the semiconductor film (not shown).

[0017] Then, a passivation film is formed on the entire surface of the lower glass substrate including the drain electrode, and the pixel electrode is electrically connected to the drain electrode through a contact hole formed on the passivation film (not shown).

[0018] In general, the number of the source and gate drivers formed varies according to resolution. In a LCD

panel of XGA (Extended graphics array) degree, eight source drivers 23 and three gate drivers 25 are required.

[0019] The source drivers 23 apply R/G/B (red/green/blue) data synchronized with the clock signals CLK applied from the timing controller 27 to each data line of the LCD panel 21.

[0020] The timing controller 27 outputs various control signals required to drive the source and gate drivers 23 and 25, and then provides data transmitted from the system (not shown) to the source drivers 23 at a rising edge timing of the clock signals CLK.

[0021] As shown in FIG. 3, the timing controller 27 provides R/G/B digital data to the source drivers 23 at the rising edge timing, and the source driver 23 samples the data at a falling edge timing of the clock signal CLK.

[0022] If the data is sampled within the source drivers 23 at the rising edge timing, the timing controller 27 provides the data to the source drivers 23 at the falling edge timing of the clock signal CLK.

[0023] Then, in the source driver 23, the digital data is converted to analog data, is constantly amplified, and then is applied to each gate line, thereby displaying the picture image by driving signals of the gate drivers.

[0024] However, the related art LCD device has the following problems.

[0025] First, the source driver connected with the data bus samples data per the falling edge timing of the data clock. At this time, unnecessary voltage is used, thereby increasing power consumption.

[0026] Furthermore, if the data is transmitted by an equal clock signal, an EMI noise emitted relatively increases, thereby degrading display quality.

SUMMARY OF THE INVENTION

[0027] Accordingly, the present invention is directed to an LCD device and a method for driving the same that substantially solves one or more problems due to limitations and disadvantages of the related art.

[0028] An object of the present invention, in part, is to provide an LCD device and a method for driving the same that can reduce power consumption during transmitting data from a timing controller to each source driver by using at least two data clock signals having different phases.

[0029] The invention, in part, pertains a LCD panel of a LCD device that displays a picture image by using a plurality of source drivers applying data signals to the LCD panel, a plurality of gate drivers applying gate driving

signals to the LCD panel, a timing controller outputting at least two clock signals having different phases and separately outputting data synchronized with each output signal, and at least two data buses transmitting the data separately output from the timing controller to the source drivers.

[0030] The invention, in part, pertains to a number of the data buses being in proportion to a number of clock signals output from the timing controller. The timing controller outputs data synchronized with a rising edge time of each clock signal, or the timing controller outputs data synchronized with a falling edge time of each clock signal. The timing controller outputs first and second clock signals having opposite phases to each other. The timing controller can also output first, second and third clock signals, each having different phases to each another.

[0031] The invention, in part, pertains to the source driver sampling data in the falling edge time when the data synchronized with the rising edge time is output. Alternatively, the source driver samples data in the rising edge time when the data synchronized in the falling edge timing is output. Odd numbered display data synchronizes with the rising edge of the first clock signal is output, and even numbered display data synchronizes with the rising

edge of the second clock signal is output. Data for displaying R color synchronizes with the rising edge of the first clock signal, data for displaying G color synchronizes with the rising edge of the second clock signal, and data for displaying B color synchronizes with the third clock.

[0032] The invention, in part, pertains to a method for driving an LCD device having a timing controller transmitting digital data received from a system to each source driver. The method includes the steps of outputting at least two clock signals having different phases, and separately outputting the digital data synchronized with respective clock signals per odd/even numbered data or R/G/B digital data through different data buses.

[0033] In the LCD device according to the present invention and the method for driving the same, the timing controller outputs at least two clock signals to source drivers, and then data synchronized with each clock signal is output to the source drivers through data buses. Accordingly, data is separately output from the timing controller to the source drivers, so that power consumption used in the timing controller and each source driver can be reduced.

[0034] It is to be understood that both the foregoing general description and the following detailed description

of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention.

[0036] FIG. 1 is a sectional view of a general LCD panel.

[0037] FIG. 2 is a schematic view showing a structure of a related art LCD device.

[0038] FIG. 3 is an operation timing view of a related art LCD device.

[0039] FIG. 4 is a schematic view of an LCD device according to the present invention.

[0040] FIG. 5 is an operation timing view of an LCD device according to an embodiment of the present invention.

[0041] FIG. 6 is a schematic view of an LCD device according to another embodiment of the present invention.

[0042] FIG. 7 is an operation timing view of an LCD device according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0043] Advantages of the present invention will become more apparent from the detailed description given herein after. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

[0044] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0045] FIG. 4 shows a block diagram of an LCD device according to an embodiment of the present invention. FIG. 5 shows an operation timing view of the LCD device according to an embodiment of the present invention showing a method for driving the LCD device of the present invention.

[0046] As shown in FIG. 4, the LCD device of the present invention includes a LCD panel 41, a plurality of source

drivers 43, a plurality of gate drivers 45, and a timing controller 47.

[0047] The plurality of source drivers 43 apply data signals to the LCD panel 41, and the plurality of gate drivers 45 apply gate driving signals to the LCD panel 41. The timing controller 47 receives a data clock signal DCLK and R/G/B digital data from a system (not shown), and outputs first and second clock signals CLK1 and CLK2 having different phases and various control signals to control the source and gate drivers 43 and 45.

[0048] At this time, the timing controller 47 is connected with each source driver by a first data bus DB1 transmitting the digital data synchronized with the first clock signal CLK1 to each source driver 43. A second data bus DB2 transmits the digital data synchronized with the second clock signal CLK2 to each source driver 43.

[0049] The R/G/B digital data is transmitted to odd numbered pixels by the first data bus DB1, and to even numbered pixels by the second data bus DB2. The phases of first and second clock signals CLK1 and CLK2 are opposite to each other.

[0050] The timing controller 47 receives the digital data from the system, synchronizes the digital data with a rising edge timing of the first clock signal CLK1, and

outputs the digital data to each source driver 43 through the first data bus DB1. Also, the digital data is synchronized with the rising edge timing of the second clock signal CLK2, and is output to each source driver 43 through the second data bus DB2.

[0051] If the timing controller 47 outputs data synchronized with the rising edge timing, each source driver 43 samples the data synchronized with a falling edge timing applied from the timing controller 47. If the source driver 43 samples data synchronized with the rising edge timing, the timing controller 47 outputs data synchronized with the falling edge timing of the first and second clock signals CLK1 and CLK2 through the first and second data buses DB1 and DB2.

[0052] As shown in FIG. 5, the R/G/B digital data, synchronized with the rising edge timing of the first clock signal CLK1 and applied to the odd numbered pixels, is transmitted to the source driver 43 through the first data bus DB1. Also, the R/G/B digital data, synchronized with the rising edge timing of the second clock signal CLK2 having an opposite phase to the first clock signal CLK1 and applied to the even numbered pixels, is transmitted to the source driver 43 through the second data bus DB2.

[0053] The timing controller 47 synchronizes digital data received from the system with two clock signals through two data buses, and then separately outputs the synchronized digital data to the source drivers. As a result, electricity used in outputting data can be reduced.

[0054] The timing controller 47 separately outputs the digital data, so that the source driver 43 separately samples the digital data. Therefore, electricity used in sampling the digital data in the source driver 43 can be reduced, thereby substantially reducing electricity for driving the whole circuit as compared to the related art.

[0055] FIG. 6 is a block diagram of a LCD device according to another embodiment of the present invention. FIG. 7 is an operation timing view of the LCD device according to another embodiment of the present invention.

[0056] In another embodiment of the present invention, three clock signals CLK1, CLK2 and CLK3 having different phases are generated. Then, a timing controller separately outputs R/G/B digital data synchronized with the each clock signal to source drivers through the first, second and third data buses DB1, DB2 and DB3.

[0057] As shown in FIG. 6, the LCD device according to another embodiment of the present invention includes an LCD

panel, a plurality of source drivers 43, a plurality of gate drivers 45, and a timing controller 47.

[0058] The plurality of source drivers 43 apply data signals to the LCD panel 41, and the plurality of gate drivers 45 apply gate driving signals to the LCD panel 41. The timing controller 47 receives data clock signal DCLK and R/G/B digital data from a system (not shown), and outputs various control signals for controlling the source and gate drivers 43 and 45 and first, second, and third clock signals CLK1, CLK2 and CLK3 having different phases.

[0059] At this time, the timing controller 47 is connected with each source driver 43 by the first, second and third data buses DB1, DB2 and DB3. The data for displaying R color synchronized with the first clock signal CLK1 is transmitted to each source driver 43 by the first data bus DB1. The data for displaying G color synchronized with the second clock signal CLK2 is transmitted to each source driver 43 by the second data bus DB2. The data for displaying B color synchronized with the third clock signal CLK3 is transmitted to each source driver 43 by the third data bus DB3.

[0060] The R/G/B digital data transmits to the timing controller 47 from the system. Then, the R/G/B digital data is synchronized with a rising edge of the first clock signal

CLK1, and then the digital data for displaying R color outputs to each source driver through the first data bus DB1. The R/G/B digital data is synchronized with the rising edge of the second clock signal CLK2, and then the digital data for displaying G color outputs to each source driver through the second data bus DB2. The R/G/B digital data is synchronized with the rising edge of the third clock signal CLK3, and then the digital data for displaying B color outputs to each source driver through the third data bus DB3.

[0061] At this time, if the timing controller 47 outputs data synchronized with the rising edge, each source driver 43 samples the data synchronized with the falling edge time and applied from the timing controller 47. If the source driver 43 samples data synchronized with the rising edge, the timing controller 47 outputs the data synchronized with the falling edge time of the first, second and third clock signals CLK1, CLK2 and CLK3 through the first, second and third data buses DB1, DB2 and DB3.

[0062] As shown in FIG. 7, in a driving circuit of the LCD device according to another embodiment of the present invention, the data for driving R color synchronized with the rising edge of the first clock signal CLK1 transmits to each source driver 43 through the first data bus DB1, and the data for driving G color synchronized with the rising

edge of the second clock signal CLK2 having a different phase to the first clock signal CLK1 transmits to the source driver through the second data bus DB2. The data for driving B color synchronized with the rising edge of the third clock signal CLK3 having a different phase to the first and second clock signals CLK2 and CLK3 is transmits to the source driver through the third data bus DB3.

[0063] That is, the timing controller 47 separately outputs digital data received from the system and synchronized with the three clock signals per the R/G/B digital data through the three data buses to each source driver, thereby reducing the electric power used in outputting the data.

[0064] Also, the timing controller 47 separately outputs digital data according to the R/G/B digital data, so that the source driver 43 separately samples the digital data according to the R/G/B digital data. Therefore, the electric power consumption for driving the whole circuit can be reduced.

[0065] As discussed above, the LCD device according to the present invention has the following advantages.

[0066] First, the timing controller separately outputs the digital data received from the system synchronized with each clock signal to the source driver through at least two

data buses, thereby reducing the electric power used in outputting the data from the timing controller to the source driver and in sampling the data in the source driver. Therefore, electricity requirement for driving the whole circuit can be reduced.

[0067] Furthermore, data is separately transmitted per odd/even numbered data or R/G/B digital data by using at least two clock signals having different phases, so that electromagnetic interference can be reduced. Therefore, it is possible to prevent degradation of the picture quality.

[0068] The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses and methods. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.